Engr433 Digital Design Autumn 2019

Text: RTL Hardware Design Using VHDL, Chu, Wiley, 2013

Note: Schedule subject to change with appropriate notice.

Date		Topic	Reading
M	Sep 23	Course Introduction; Review - Combinational logic, K-maps	Notes
Tu	24	Lab1: Digital Noise	
W	25	Review - Entered Variable Mapping, MSI functions	Notes
F	27	Review - Sequential Logic, Latches, Flip-Flops	Notes
M	30	Review - State Machine Design **(9:50)**	Notes
Tu	Oct 1	Lab2: State Machine Design **(2:30)**	
W	2	Review - State Machine Design **(9:50)**	Notes
F	4	Alternative State Machine Architectures **(9:50)**	Notes
M	7	Alternative State Machine Architectures; Asynchronous Inputs	Notes
Tu	8	Lab3: Schematic-driven FPGA Implementation – Basic	
W	9	Implementation Strategies; Test Review	Notes
F	**11**	**Mid-term #1**	
M	**14**	**Senior Trip – No Class**	
Tu	**15**	**Senior Trip – No Lab**	
W	**16**	**Service Day – No Class**	
F	18	Counters and Registers	Notes
M	21	Xilinx Spartan 6 FPGA Architecture; Introduction to Digital System Design	Notes, Chapter 1
Tu	22	Lab4: Schematic-driven FPGA Implementation – Advanced	
W	23	Overview of Hardware Description Languages	Chapter 2
F	25	Basic Language Constructs of VHDL	Chapter 3
M	28	In-class Exercise – 4-bit Adder Design Using VHDL	
Tu	29	Lab5: VHDL Synthesis – Combinational Applications	
W	30	Concurrent Signal Assignment Statements of VHDL	Chapter 4
F	Nov 1	Sequential Statements of VHDL	Chapter 5
M	4	In-class Exercise – State Machine Design Using VHDL	
Tu	5	Lab6: VHDL Synthesis – Sequential Applications	
W	6	Project Background	Notes
F	8	Project Discussion	Notes
M	11	Project Issues	Notes
Tu	12	Lab7: Project Work	
W	13	Project Brainstorming	
F	15	Project Meetings as Necessary	
M	18	Video – Silicon Run I	
Tu	19	Lab8: Project Work	
W	20	Project Consulting	
F	22	No Class	
	24-30	Thanksgiving Vacation	
M	Dec 2	Project Meetings as Necessary	
Tu	3	Lab9: Project Work	
W	4	Project Meetings as Necessary	
F	6	Conclusions and Evaluation	
W	**Dec 11**	**Final Exam Time (8:00 - 9:50am)**	Project Checkout